TM 11-5895-244-10

DEPARTMENT OF THE ARMY TECHNICAL MANUAL

OPERATOR'S MANUAL

TEST SET
ELECTRONIC CIRCUIT
PLUG-IN UNIT
TS-1209/MSQ

HEADQUARTERS, DEPARTMENT OF THE ARMY
NOVEMBER 1959

AGO 2502A—Nov

WARNING

Be careful when working on power connections.
Serious injury or death may result from
contact with these terminals.

TECHNICAL MANUAL

Operator's Manual

TEST SET, ELECTRONIC CIRCUIT PLUG-IN UNIT TS-1209/MSQ

TM 11-5895-244-10
CHANGES No. 1

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON 25, D .C., *17 March 1960*

TM 11-5895-244-10, 6 November 1959, is changed as follows:

Page 28. Add the following appendix after chapter 5.

APPENDIX

BASIC ISSUE ITEMS

(Added)

1. Scope

a. This appendix lists items supplied for initial operation and for running spares. The list includes accessories issued as part of the major end item. End items of equipment are issued on the basis of allowances prescribed in the equipment authorization tables and other documents that are a basis for requisitioning.

b. Columns are described as follows:

(1) *Source, maintenance, and recoverability code.* Not used.

(2) *Federal stock number.* The stock number column lists the 11-digit Federal stock number.

(3) *Designation by model.* When a dagger symbol (†) is placed in column 3, it indicates the model in which the part is used.

(4) *Description.* Nomenclature or the standard item name and brief identifying data for each item is listed in this column. When requisitioning, enter the nomenclature and description on the requisition.

(5) *Unit of issue.* The unit of issue is the supply medium by which the individual item is counted for procurement, storage, requisitioning, allowances, and issue purposes.

(6) *Expendability.* Expendable items are indicated by the letter X; nonexpendable items are indicated by NX.

(7) *Quantity authorized.* Under "Items Comprising an Operable Equipment" the column lists the quantity of items supplied for the initial operation of the equipment.

(8) *Illustration.* Not used.

2. Part Numbers

If no stock number appears in column 2, an applicable stock number is in the process of assignment. In approximately 90 days, a change will be issued indicating the appropriate stock numbers for requisitioning purposes. The Hughes Aircraft Co. part number which appears in the description column, has been included and may be used in emergencies to identify items.

3. Comments or Suggestions

Any comments concerning omissions and discrepancies in this manual will be prepared on DA Form 2028 and forwarded direct to Commanding Officer, U.S. Army Signal Equipment Support Agency, Fort Monmouth, N. J., ATTN: SIGFM/ES-ML.

(1) SOURCE MAINTENANCE AND RECOVERABILITY CODE	(2) FEDERAL STOCK NUMBER	(3) DESIGNATION BY MODEL	(4) DESCRIPTION	(5) UNIT OF ISSUE	(6) EXPENDABILITY	(7) QUANTITY AUTHORIZED	(8) ILLUSTRATIONS FIGURE NO	(9) ILLUSTRATIONS ITEM NO
		1 2	ITEMS COMPRISING AN OPERABLE EQUIPMENT					
			TEST SET, ELECTRICAL CIRCUIT, PLUG-IN TS-1209/MSQ					
			NOTE: Model Column No. 1 refers to the Development Model, Order No.22833-PH-54; Column 2 refers to the Production Model, Order No. 19001-PH-59.					
	5895-705-9155	† †	TEST SET, ELECTRICAL CIRCUIT, PLUG-IN TS-1209/MSQ: HAC dwg No. X503096-100; No. 503096-101	ea	NX			
	5995-686-4455	† †	CABLE ASSEMBLY, POWER, ELECTRICAL: 3 ft 6 in lg 1/a; HAC part/dwg No. 534911	ea	X	1		
		† †	CABLE ASSEMBLY, RADIO FREQUENCY: 5 ft 2 in lg o/a; HAC part/dwg No. 535149	ea	X	1		
			RUNNING SPARES AND ACCESSORY ITEMS					
			TEST SET, ELECTRICAL CIRCUIT, PLUG-IN TS-1209/MSQ					
			NO PARTS AUTHORIZED FOR STOCKAGE AT FIRST ECHELON					

By Order of *Wilber M. Brucker*, Secretary of the Army:

L. L. LEMNITZER,
General, United States Army,
Chief of Staff.

Official:
The Adjutant General.
Major General, United States Army,
R. V. LEE,

Distribution:

Active Army:

USASA (2)
CNGB (1)
Technical Stf, DA (1)
except CSigO (18)
Technical Stf, Bd (1)
USCONARC (5)
USA Arty Bd (1)
USA Armor Bd (1)
USA Armor Bd Test Sec (1)
USA Inf Bd (1)
USA Air Def Bd (1)
USA Air Def Bd Test Sec (1)
USA Abn & Elct Bd (1)
USA Avn Bd (1)
USA Arctic Test Bd (1)
US ARADCOM (2)
US ARADCOM Rgn (2)
OS Maj Comd (5)
OS Base Comd (5)
Log Comd (5)
MDW (1)
Armies (5) except First US
Army (7)
Corps (2)
Div (2)
USATC (2)
Ft. Belvoir (5)
Def Atomic Spt Agcy (5)
Yuma Test Sta (2)
USA Elect PG (1)
Svc Colleges (5)
Br Svc Sch (5) except
USASCS (25)
Sig Sec, Gen Depot (12)
GENDEP (2)
Sig Dep (19)
AFIP (1)
WRAMC (1)
AMS (1)
Engr Maint Cen (1)
USA Comm Agcy (2)
USA Sig Comm Engr Agcy (1)
USA Sig Eqp Spt Agcy (2)
USA Sig Msl Spt Agcy (1)
Trans Terminal Comd (1)
Army Terminals (1)
Port of Emb (OS) (2)
OS Sup Agcy (1)
Sig Fld Maint Shops (3)
Sig Lab (5)
USA Corps (Res) (1)
USASSA (15)
Midwestern Rgn Ofc (USASSA) (1)
JBUSMC (2)
USA Sig Pubs Agcy (8)
Army Pictorial Cen (2)
USA Ord Msl Comd (3)

Units org under fol TOE:

11-7 (2)
11-16 (2)
11-57 (2)
11-98 (2)
11-117 (2)
11-155 (2)
11-500 (AA-AE) (2)
11-557 (2)
11-587 (2)
11-592 (2)
11-597 (2)

NG: State AG (3); units—same as Active Army except allowance is one copy to each unit.
USAR: None.
For explanation of abbreviations used, see AR 320-50.

☆U. S. GOVERNMENT PRINTING OFFICE: 1960—520797/1578

TECHNICAL MANUAL
No. 11–5895–244–10

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON 25, D. C., *6 November 1959*

TEST SET, ELECTRONIC CIRCUIT PLUG-IN UNIT TS–1209/MSQ

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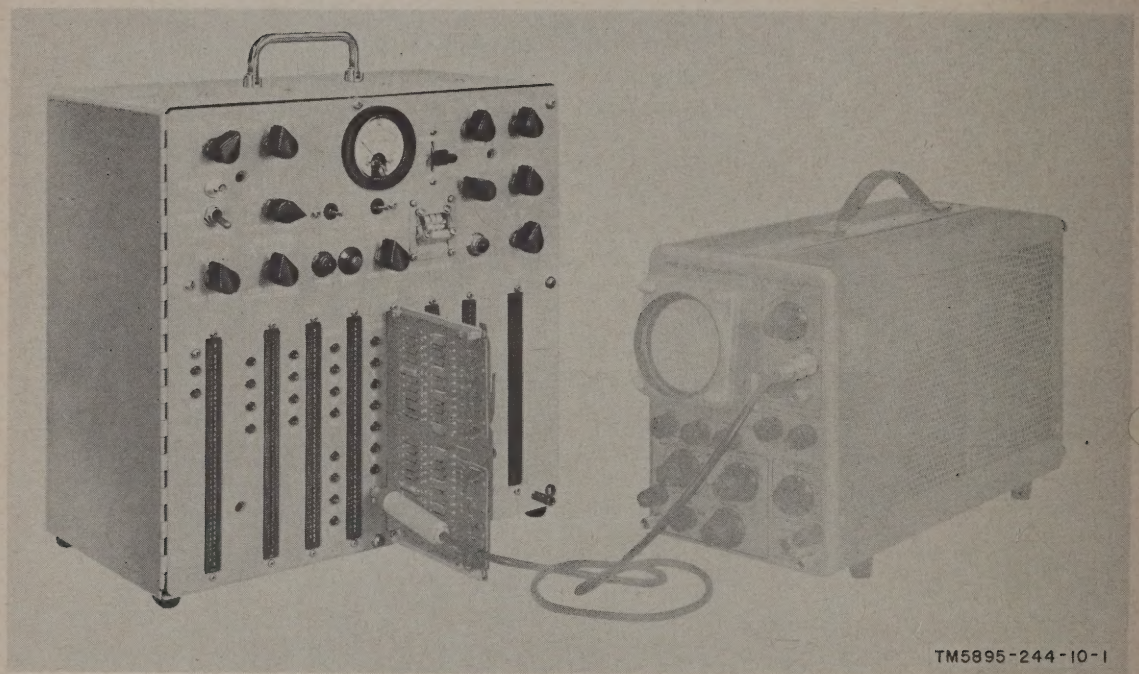


Figure 1. Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ, test bench application.

CHAPTER 1
INTRODUCTION

Section I. GENERAL

1. Scope

a. This manual describes Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ, and covers installation, operation, and operator's maintenance.

b. The maintenance allocation chart will appear in the organizational maintenance manual.

2. Forms and Records

a. Electronic Failure Reports. Fill out and forward DD Form 787–1 (Electronic Failure Report) to the Commanding Officer, U. S. Army Signal Equipment Support Agency, Fort Monmouth, N. J. as prescribed in AR 700–39.

b. Report of Damaged or Improper Shipment. Fill out and forward DD Form 6 (Report of Damaged or Improper Shipment) as prescribed in AR 700–58.

c. Preventive Maintenance Forms. Prepare DA Form 11–266 (figs. 8 and 9) (Maintenance Check List for Signal Equipment (Test Equipment)) in accordance with instructions on the form.

d. Parts List Form. Forward DA Form 2028 (Recommended Changes to DA Technical Manual Parts List or Supply Manuals 7, 8, and 9) directly to the Commanding Officer, U. S. Army Signal Equipment Support Agency, Fort Monmouth, N. J., with comments on part listings.

e. Comments on Manual. Forward all other comments on this publication to the Commanding Officer, U. S. Army Signal Publication Agency, Fort Monmouth, N. J.

Section II. DESCRIPTION AND DATA

3. Purpose and Use

Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ is an item of special test equipment supplied with each subsystem vehicle of the AN/MSQ–18 system. Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ consists of a single unit and is used to test standard digital plug-in circuit cards (par. 7) installed within the components of a subsystem. Test results and indications are obtained with a panel meter, an indicator lamp, or an external oscilloscope. (All six-digit assembly numbers used in this publication are Hughes Aircraft Company assembly numbers.)

4. Technical Characteristics

Internal clock pulse generator output:	
Amplitude	6 volts.
Polarity	Negative.
Pulse width	1.3 msec no load, .9 msec with load.
Pulse spacing	20 ±.2 msec.
Pulse repetition frequency.	50 kc.
Internal flip-flop output:	
Amplitude	6 volts.
Polarity	Negative.
Rise time	.2 to .35 msec.
Fall time	.1 to .3 msec.
Panel meter	0 to 20 microamperes.
Power requirements	6.3 vac ±.3 volt, 60 cps, ac; +1.5 ±.07 volt dc; +28 ±1.4 volts dc; +150 ±7.5 volts dc; —6 ±.3 volt dc; —7.5 ±1.4 volts dc; —28 ±1.4 volts dc; —150 ±7.5 volts dc.

5. Table of Components (fig. 2)

a. The table of components is as follows:

Quantity	Component	Height (in.)	Depth (in.)	Width (in.)	Weight (lb)	Length (in.)
1	Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ, including:	15.75	10	15	33	
1	JK medium flip-flop test assembly 540013	5.13	.75	7.63	¾	
1	Cable assembly, power 534911				3	36
1	Cable assembly, coaxial 535149				1	60

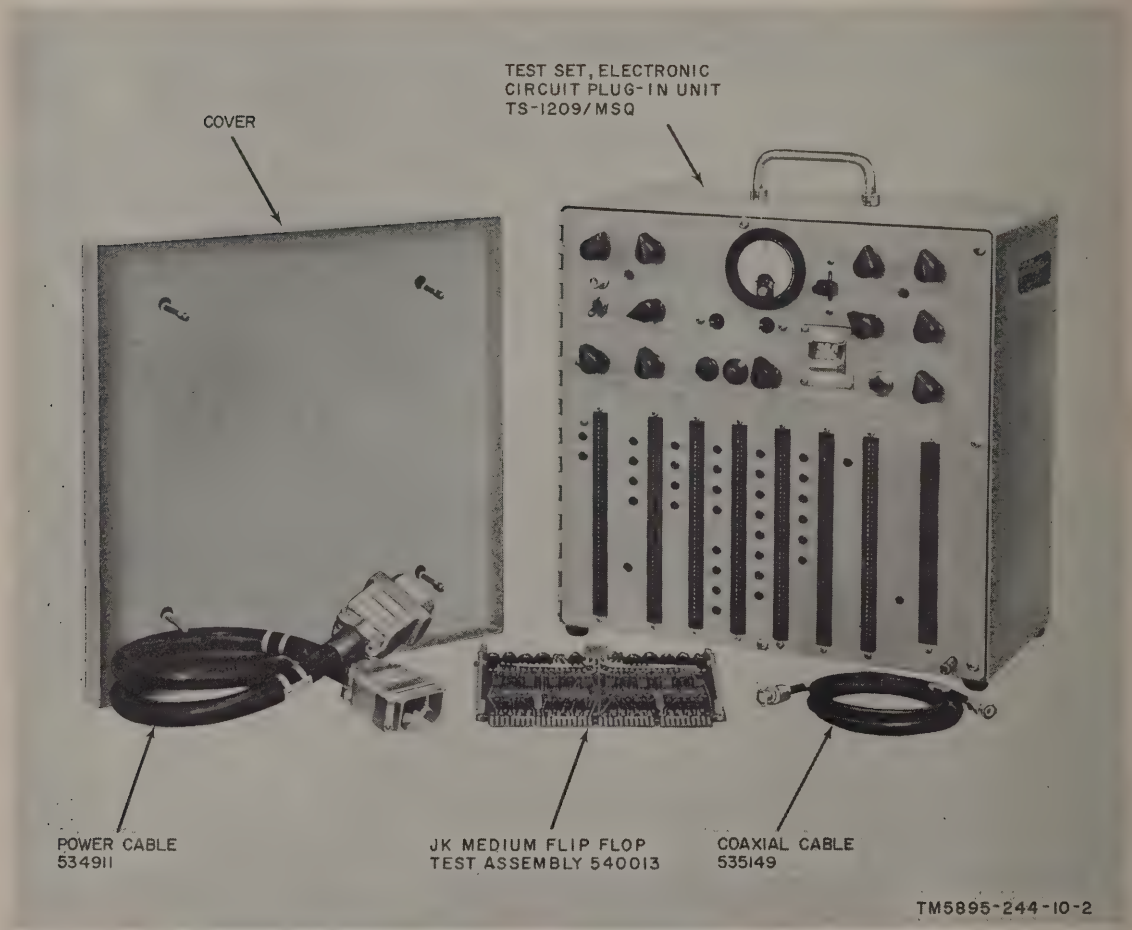


Figure 2. Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ, components.

b. Running spares for Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ are included in the running spares of the associated AN/MSQ–18 subsystem.

6. Common Names

Designation	Common name
Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ.	Test set
JK medium flip-flop test assembly 540013.	Transistor dynamic test card.
Cable assembly, power 534911	Power cable
Cable assembly, coaxial 535149	Trigger cable
Oscilloscope AN/USM–89	Oscilloscope
Multimeter AN/URM–105	Multimeter

Note. The oscilloscope and multimeter are used with, but are not a part of, the test set.

7. Description of Test Set

a. The test set (fig. 2) provides a means of testing any one of 14 standard digital plug-in circuit cards and elements, which is suspected of trouble. The standard digital plug-in circuit cards are as follows:

(1) JK low flip-flop 530225
(2) JK medium flip-flop 530226
(3) K$\overline{K}$ flip-flop 530227
(4) Clock pulse generator 532465
(5) Core register 9A 531783
(6) Core register 9B 531784
(7) Core register 10A 531781
(8) Core register 10B 531782
(9) Core driver 530842
(10) Emitter follower 531706
(11) Negator 531137
(12) Diode card 531723
(13) Individual transistors
(14) Individual diodes

b. All of the operating controls, the panel meter, and the error indicator lamp are located on the front panel. The test jacks on the front panel hold the suspected plug-in circuit card during test. The test points are provided to make test measurements of the suspected card, using external test equipment. A synchronizing trigger signal for external equipment may be obtained from a jack on the front panel. The power cable is connected at the rear of the test set.

8. Description of Minor Components

The minor components of Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ are shown in figure 2. Some of the features of the minor components are as follows:

a. JK medium flip-flop test assembly 540013 is a modified JK medium power flip-flop assembly into which individual transistors may be installed for dynamic testing (testing under load). During operation, modified JK medium power flip-flop test assembly 540013 is plugged into the F/F test jack on the front panel of the test set.

b. Coaxial cable assembly 535149 is 60 inches long and is equipped with a UG–260B/U coaxial plug at each end. This cable is used to carry an internally generated trigger to an external unit for synchronizing purposes.

c. Power cable assembly 534911 is 36 inches long, and has a multiconductor connector at each end. This cable is used to apply power from the SYSTEMS TEST VOLTAGES jack on the maintenance bench to the test set.

CHAPTER 2
INSTALLATION

Section I. SERVICE UPON RECEIPT OF EQUIPMENT

9. Unpacking

a. No special unpacking procedures are required for Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ, since the test set is shipped inside Operations Central AN/MSQ–18 (OC) or Coder-Decoder Group OA–1593/MSQ–18 (CDG). The test set is stored in the storage cabinets in the OC and the CDG and is held in place with web tiedown straps (fig. 3).

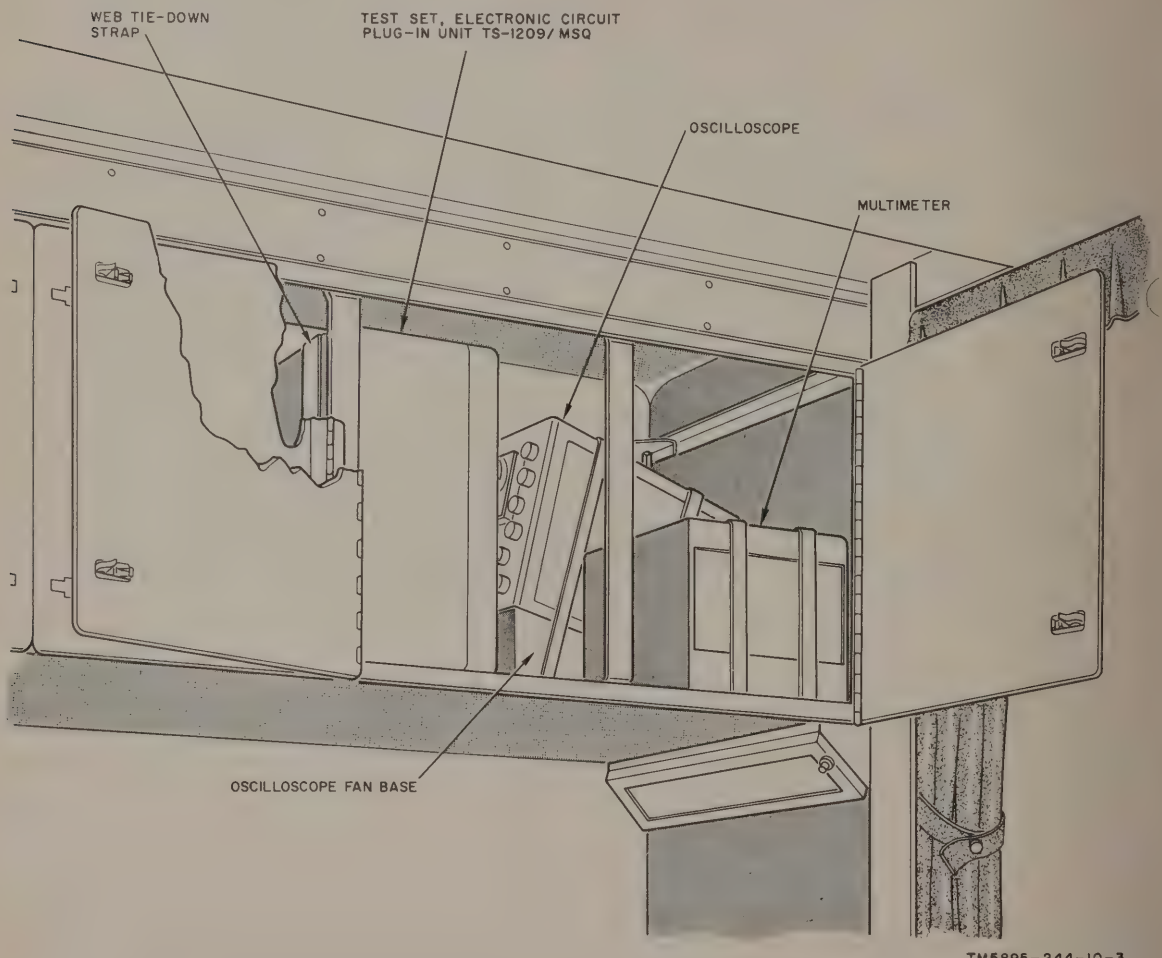


Figure 3. Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ, storage when not in use.

b. To remove the test set from its storage space, open the cabinet doors and remove the tiedown straps. Remove the test set from the cabinet and place it in a convenient position on the maintenance bench.

10. Checking Unpacked Equipment

a. Inspect the test set for damage incurred during shipment. If the test set has been damaged, refer to paragraph 2*b*.

b. Check the test set against the table of components (par. 5).

Note. The power and trigger cables are stored in the rear compartment of the test set. The transistor dynamic test card is stored in clip fasteners inside the cover.

11. Test Equipment Required for Installation

Test equipment which is required for initial adjustment of the test set is supplied with Operations Central AN/MSQ–18 (OC) or Coder-Decoder Group OA–1593/MSQ–18 (CDG). This test equipment consists of Oscilloscope AN/USM–89 and Multimeter AN/URM–105.

12. Installation

Place the test set on the maintenance bench and remove the cover. Make the connections listed in the following chart. These connections are also shown in figure 4.

Cable connections

Cable No.	Cord	Required No.	Length (in.)	Connects	
				From	To
	Cable assembly, power 534911	1	36	SYSTEMS TEST VOLTAGES jack on maintenance bench.	Power jack J3 of test set (fig. 5).
	Cable assembly, coaxial, 535149.	1	60	Trigger input jack of the oscilloscope.	TRIGGER OUT jack J104 of test set.

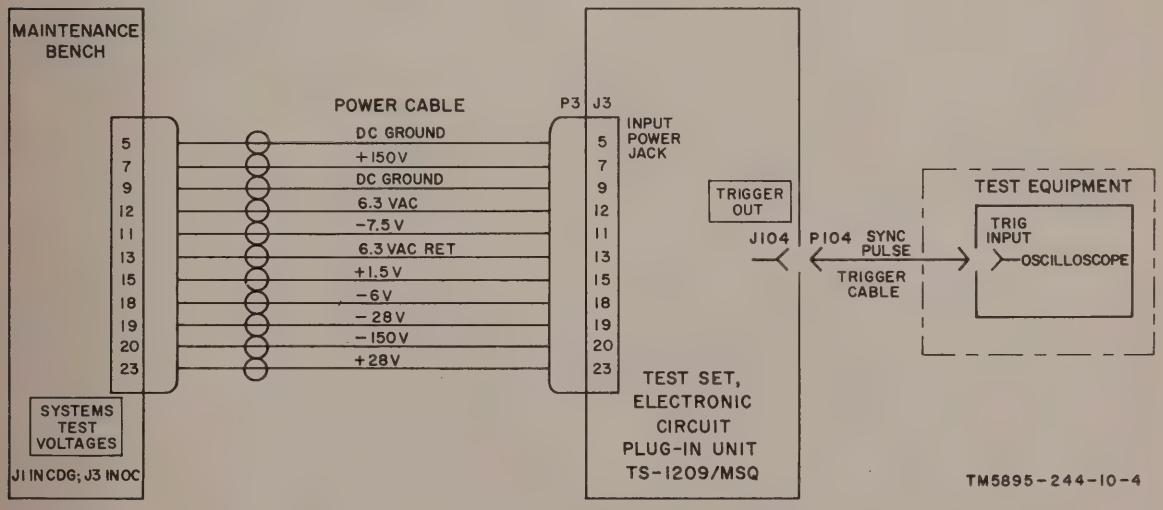


Figure 4. Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ, cording diagram.

Section II. INITIAL ADJUSTMENTS

Note. The procedures described in this section should be performed by personnel familiar with the use of controls and operating procedures of the test set. Before performing the checks and adjustments listed below, connect the power cable as specified in paragraph 12. Operating controls are listed and described in paragraph 21.

13. Input Voltage Checks (fig. 5)

Perform the preliminary starting procedures given in paragraph 23 and check the input voltages as listed below.

a. Set the POWER switch to ON.

b. Measure +150 ±7.5 volts dc between TP603 and ground.

c. Measure +28 ±1.4 volts dc between TP610 and ground.

d. Measure +1.5 ± .07 volt dc between TP606 and ground.

e. Measure —6 ± .3 volt dc between TP607 and ground.

f. Measure —7.5 ±1.4 volts dc between TP604 and ground.

g. Measure —28 ±1.4 volts dc between TP608 and ground.

h. Measure —150 ±7.5 volts dc between TP609 and ground.

i. Measure 6.3 ±.3 volt ac between TP605 and TP611.

j. Set the POWER switch to OFF.

14. Diode Reverse Test Adjustments

a. Set the POWER switch to ON.

b. Set the TRANSISTOR - OFF - DIODE switch to DIODE.

c. Set the DIODE switch to REV.

d. Set the TENS switch to 3.

e. Set the UNITS switch to 3.

f. The panel meter should read 5 microamperes.

g. If the panel meter does not read 5 microamperes, adjust E REF REVERSE potentiometer R409 (fig. 5) to obtain a 5-mocroampere reading.

h. Set the POWER switch to OFF.

15. Diode Forward Test Adjustments

a. Set the POWER switch to ON.

b. Set the TRANSISTOR - OFF - DIODE switch to DIODE.

c. Set the DIODE switch to FWD.

d. Set the TENS switch to 3.

e. Set the UNITS switch to 2.

f. Connect the multimeter to measure positive 1 volt dc between TP401 and ground (fig. 5).

g. Adjust 1 REF FORWARD potentiometer R405 (fig. 5) to obtain 1 volt on the multimeter.

h. Disconnect the multimeter from TP401 and ground.

i. Adjust METER CALIB potentiometer R407 to obtain a 10-microampere reading on the panel meter.

j. Set the POWER switch to OFF.

16. Transistor Test Adjustments

a. Set the POWER switch to ON.

b. Set the TRANSISTOR - OFF - DIODE switch to TRANSISTOR.

c. Set the TRANSISTOR switch to CALIB.

d. The panel meter should read 10 microamperes.

e. If the panel meter does not read 10 microamperes, adjust TRANS E. ADJ. potentiometer R402 (fig. 5) to obtain a 10-microampere reading.

f. Set the POWER switch and TRANSISTOR-OFF-DIODE switch to OFF.

17. Clock Pulse Generator Test Adjustments

a. Set IN-OUT switch S601 (fig. 5) to OUT.

b. Set the POWER switch to ON.

c. Observe the waveform shown in E, figure 7, at TP601 (fig. 5). If incorrect, higher echelon adjustment is required.

d. Set the IN-OUT switch (fig. 5) to ON.

e. Observe the waveform at TP601 and adjust potentiometer R628 for a pulse amplitude of 1.8 volts.

f. Disconnect the oscilloscope from TP601.

g. Set the IN-OUT switch to OUT.

h. Set the POWER switch to OFF.

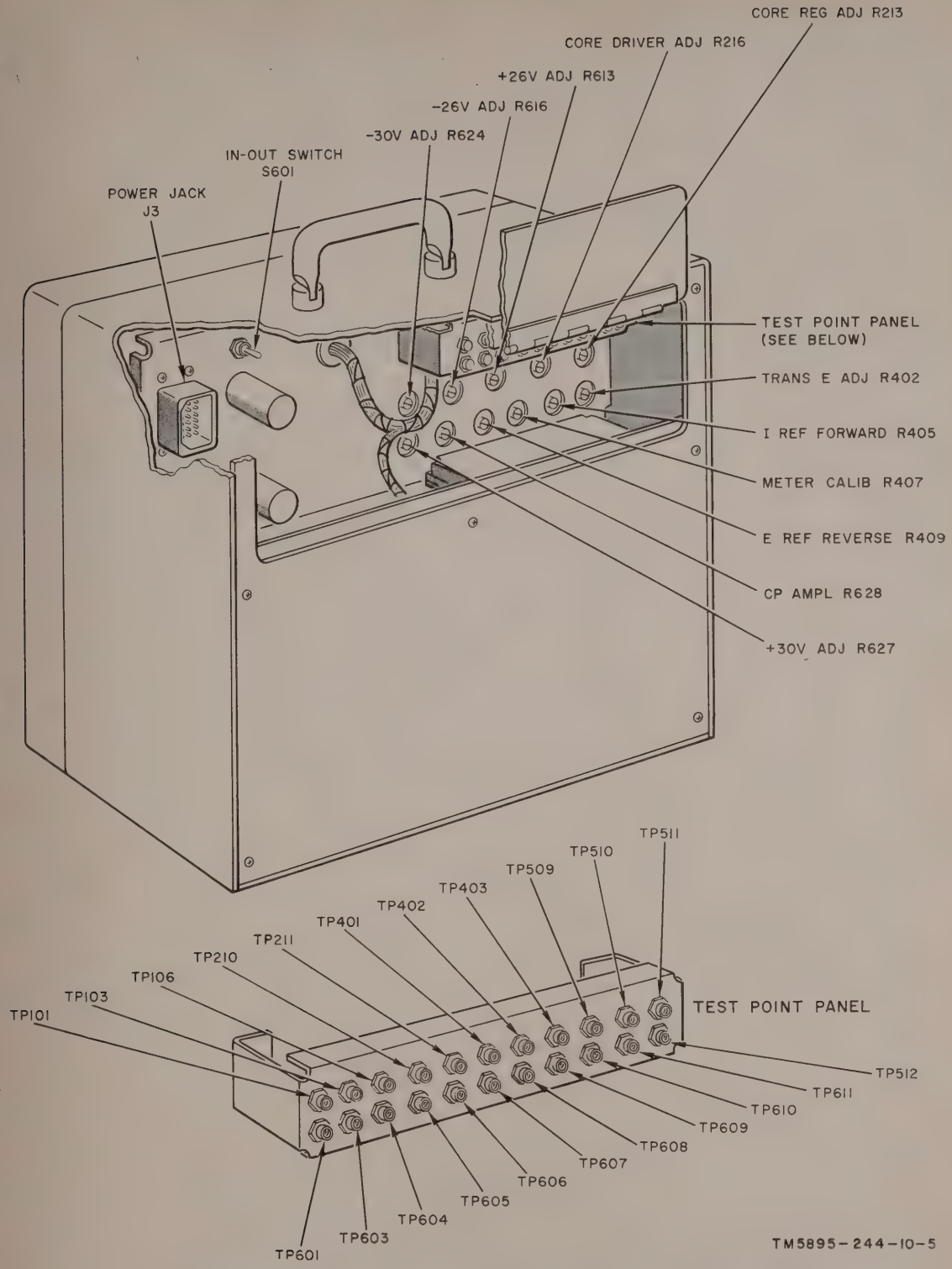


Figure 5. Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ, adjustments and test points.

18. Core Register Test Adjustments

Note. This adjustment requires a core register card 9B 531784 which is known to be good. This card may be obtained from running spares or an operable AN/MSQ-18 equipment.

a. Install core register 9B 531784 into C/RB test jack on the front panel.

b. Set the POWER switch to ON.

c. Set the CORE REGISTER & CONDITION SELECTOR switch to 9 BIT–2.

d. Adjust CORE REG ADJ potentiometer R213 to obtain the waveform shown in 0, figure 7, at TP210 (fig. 5).

e. Set the POWER switch to OFF.

19. Core Driver Test Adjustments

Note. This adjustment requires a core driver card 530842 which is known to be good. This card may be obtained from running spares or an operable AN/MSQ–18 equipment.

a. Install core driver 530842 into CD test jack on the front panel.

b. Set the POWER switch to ON.

c. Set the CONDITION switch to NORM.

d. Adjust CORE DRIVER ADJ potentiometer R216 (fig. 5) to obtain +140 volts dc at pin $\bar{y}$ of the CD test jack.

e. Set the POWER switch to OFF.

20. Flip-Flop Test Adjustments (fig. 5)

a. Set the POWER switch to ON.

b. Adjust +30V ADJ potentiometer R627 to obtain +30.4 volts dc at TP509.

c. Adjust —26V ADJ potentiometer R616 to obtain —26.3 volts dc at TP510.

d. Adjust +26V ADJ potentiometer R613 to obtain +26.3 volts dc at TP511.

e. Adjust —30V ADJ potentiometer R624 to obtain —30.4 volts dc at TP512.

f. Set the POWER switch to OFF.

CHAPTER 3
OPERATING INSTRUCTIONS

21. Operating Controls, Indicators, Jacks, and Test Points (fig. 6)

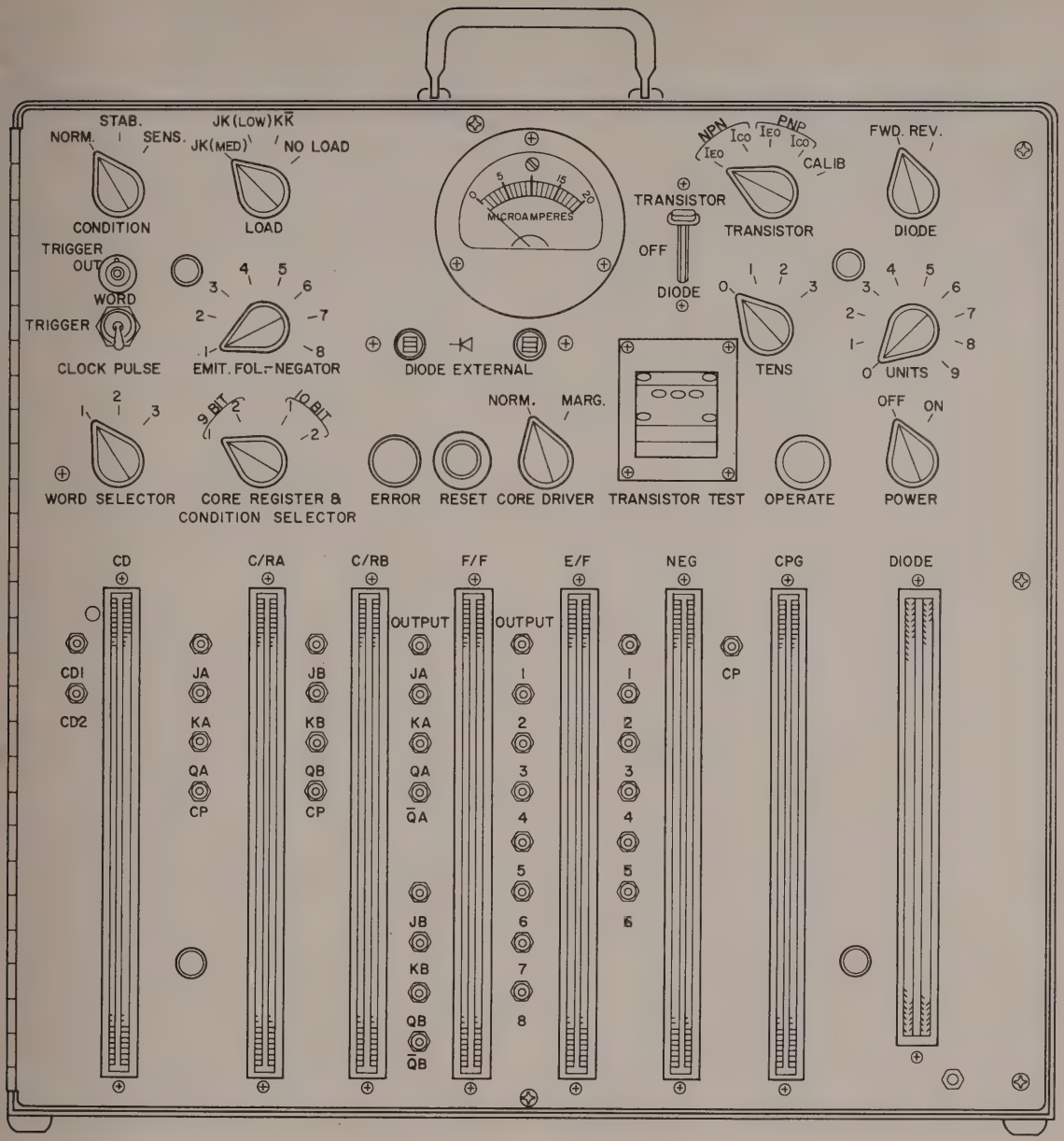
The operating controls, indicators, jacks, and test points and their functions are listed in table I.

Table I. Operating Controls, Indicators, Jacks, and Test Points

Control, indicator, jack or test point	Function
POWER switch	Turns the test set on or off.
OPERATE pilot lamp	Lights when test set is turned on.
TENS switch	Selects groups of diodes for test on diode cards 531723. In group 0 position, permits selection of diodes A, B, E, F, H, J, K, L, and M. In group 1 position, permits selection of diodes R, S, T, V, W, X, A, B, C, and D. In group 2 position, permits selection of diodes E, F, H, L, M, N, P, R, S, and T. In group 3 position, permits selection of diodes X, Y, external (individual) and panel meter check.
UNITS switch	Selects individual diodes of the group selected by the TENS switch. When the TENS switch is in 3 position, 2 and 3 positions of the UNITS switch allow panel meter checking and calibration. With TENS switch in 3 position and UNITS switch in 4 position, individual diodes may be tested.
DIODE switch	In FWD. position, provides testing diode current in forward direction (conduction). In REV. position, allows reverse current check of diode under test.
TRANSISTOR switch	In NPN-I_{EO} position, allows measurement of emitter-base current of NPN type transistor. In NPN-I_{CO} position, allows measurement of collector-base current of NPN type transistor. In PNP-I_{EO} position, allows measurement of emitter-base current of PNP type transistor. In PNP-I_{CO} position, allows measurement of collector-base current of PNP type transistor. In CALIB position, permits checking of panel meter for transistor testing.
TRANSISTOR-OFF-DIODE switch	In TRANSISTOR position, connects panel meter to transistor test circuits. In OFF position, disconnects panel meter from both transistor and diode test circuits. In DIODE position, connects panel meter to diode test circuits.
TRANSISTOR TEST socket	Accepts and holds both PNP and NPN type transistors for static testing.
CORE DRIVER switch	In NORM. position, provides normal clock pulse input of $-6 \pm .3$-volt amplitude to core driver under test. In MARG. position, provides marginal clock pulse input of $-4.5 \pm .44$-volt amplitude to core driver under test.
Panel meter	Indicates current measurements from 0 to 20 microamperes of transistors and diodes under test.
RESET switch	Turns off ERROR lamp when pressed during core register test.
ERROR lamp	Lights during core register test operation to indicate error in core register under test. Remains on during all other modes of operation.
DIODE EXTERNAL test socket	Accepts and holds individual diodes for testing.
CORE REGISTER & CONDITION SELECTOR switch.	In 9 BIT-1 position, provides normal 150 volts to nine bit core register under test. In 9 BIT-2 position, provides stabilized 140 volts to nine bit core register under test. In 10 BIT-1 position, supplies normal 150 volts to 10 bit register under test. In 10 BIT–2 position, supplies stabilized 140 volts to 10 bit core register under test.

Table I. Operating Controls, Indicators, Jacks, and Test Points—Continued

Control, indicator, jack or test point	Function
EMIT. FOL.-NEGATOR switch	In positions 1 through 8, selects individual emitter follower or negator circuits of the emitter follower or negator card under test. Since only six negator circuits are mounted on one card, positions 7 and 8 are blank during negator test.
LOAD switch	In JK (MED) position, applies 35-milliampere load in —6-volt state and 29-milliampere load in 0-volt state for flip-flop under test. In JK (LOW) position, applies 10-milliampere load in —6-volt state and 8.2-milliampere load in 0-volt state for flip-flop under test. In K$\overline{K}$ position, provides 10-milliampere load in —6-volt state and 8.2-milliampere load in 0-volt state for flip-flop under test. In NO LOAD position, flip-flop under test is operated with no output load.
WORD SELECTOR switch	In position 1, selects 101010101010 word pattern for core register testing. In position 2, selects 000001000000 word pattern for core register testing. In position 3, selects 111110111111 word pattern.
TRIGGER switch	In CLOCK PULSE position, clock pulse is made available at TRIGGER OUT jack on front panel. In WORD position, word pattern of 100000000000 is available at TRIGGER OUT jack.
TRIGGER OUT jack	(Same as above)
CONDITION switch	In NORM position, supplies normal clock pulses, +28 volts dc, and —28 volts dc to flip-flop under test. In STAB position, supplies marginal clock pulses, +26.3 ±1.3 volts dc, and —30.4 ±1.5 volts dc to flip-flop under test. In SENS position, supplies below margin clock pulses, +30.4 ±1.5 volts dc, and —26.5 ±1.3 volts dc to flip-flop under test.
CD test jack	Accepts and holds core driver card for testing.
Test points CD1 and CD2	Provide means of observing and checking output of core driver card under test.
C/RA test jack	Accepts and holds 9- and 10-bit A model core register cards for testing.
Test points JA, KA, QA, and CP	Test points JA and KA provide means of observing and checking outputs of core register card under test. Test point QA provides means of observing and checking input to core register under test. Test point CP provides means of observing clock pulse input to core register card under test.
C/RB test jack	Accepts and holds 9- and 10-bit B model core register cards for testing.
Test points JB, KB, QB, and CP	Test points JB and KB provide means of observing and checking outputs of core register card under test. Test point QB provides means of observing and checking input to core register card under test. Test point CP provides means of observing and checking clock pulse input to core register under test.
F/F test jack	Accepts and holds JK low power, JK medium power, and K$\overline{K}$ flip-flop cards for testing.
Test points OUTPUT JA, KA, QA, $\overline{Q}$A, and test points JB, KB, QB, and $\overline{Q}$B.	Test points JA and KA provide means of observing and checking inputs to A section of flip-flop card under test. Test points QA and $\overline{Q}$A provide means of observing and checking the A section outputs of flip-flop card under test. Test points JB, KB, QB, and $\overline{Q}$B are used to make identical observations and checks on B section as are made on A section of flip-flop card under test.
E/F test jack	Accepts and holds emitter follower card for testing.
Test points OUTPUT 1, 2, 3, 4, 5, 6, 7, and 8.	Provide means of observing and checking outputs of each emitter follower circuit of emitter follower card under test.
NEG test jack	Accepts and holds negator card for testing.
Test points 1, 2, 3, 4, 5, and 6	Provide means of observing and checking outputs of each negator circuit on negator card under test.
CPG test jack	Accepts and holds clock pulse generator card for testing.
Test point CP	Provides means of observing and checking output of clock pulse generator card under test.
DIODE test jack	Accepts and holds diode card for testing.



TM5895-244-10-6

Figure 6. Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ, operating controls, jacks, and test points.

22. Types of Operation

Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ is used to test standard digital plug-in circuit cards and individual diodes and transistors of the AN/MSQ–18 system. The different types of standard digital elements that may be tested are as follows:

JK low, JK med, or K$\bar{K}$ flip-flop (par. 24).
Clock pulse generator (par. 25).
Core register 9A (par. 26).
Core register 10A (par. 27).
Core register 9B (par. 28).
Core register 10B (par. 29).
Core driver (par. 30).

Emitter follower (par. 31).
Negator (par. 32).
Diode card (par. 33).
Individual diodes (par. 34).
Transistors (dynamic test) (par. 35).
Transistors (static test) (par. 36).

23. Preliminary Starting Procedure

(fig. 5)

Perform the preliminary operations listed below before operating the test set as described in paragraphs 24 through 36.

a. Set the POWER switch to OFF.

b. To connect the test set in the OC:

(1) Depress the TEST BENCH POWER-OFF switch S3 on ac protective panel 503406.

(2) Connect the power cable to power jack J3 on the test set and to SYSTEMS TEST VOLTAGES jack J3 on the maintenance bench (par. 12).

(3) Check to see that STANDBY POWER CONTROL circuit breaker CB2 on ac protective panel 503406 is in the ON position.

(4) Depress TEST BENCH POWER-ON switch S2 on ac protective panel 503406.

c. To connect the test set in the CDG:

(1) Set the load ON-OFF switch S2 on power control panel 504306 to OFF.

(2) Connect the power cable to power jack J3 on the test set and to SYSTEMS TEST VOLTAGES jack J1 on the maintenance bench (par. 12).

(3) Set the load ON-OFF switch S2 on power control panel 504306 to ON.

24. Flip-Flop Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for flip-flop testing.

Note. The following steps are performed for testing JK low power 530225, JK medium power 530226, and $K\overline{K}$ 530227 flip-flop cards.

a. Connect the trigger cable from the TRIGGER OUT jack on the test set to the trigger input jack on the oscilloscope.

b. Place the flip-flop card to be tested into the F/F test jack on the front panel of the test set.

c. Set the LOAD switch to a position corresponding to the type of flip-flop that is under test; JK (LOW), JK (MED), $K\overline{K}$, or NO LOAD (if desired).

d. Set the IN-OUT switch to OUT.

e. Set the CONDITION switch to NORM.

f. Set the POWER switch to ON. See that the OPERATE and ERROR lamps light.

g. Set the TRIGGER switch to CLOCK PULSE, and synchronize the oscilloscope.

h. Insert the oscilloscope probe into the test point JA and refer to A, figure 7, for the required waveform characteristics.

i. Repeat step *h* above for test point JB.

j. Insert the oscilloscope probe into test point KA and refer to B, figure 7, for the required waveform characteristics.

k. Repeat step *j* above for test point KB.

l. Insert the oscilloscope probe into test point QA and refer to C, figure 7, for the required waveform characteristics.

m. Repeat step *l* above for the test point QB.

n. Insert the oscilloscope probe into test point $\overline{Q}$A and refer to D, figure 7, for the required waveform characteristics.

o. Repeat step *n* above for test point $\overline{Q}$B.

p. Set the CONDITION switch to STAB.

q. Repeat steps *h* through *o* above.

r. Set the CONDITION switch to SENS.

s. Repeat steps *h* through *o* above. See that the A and B flip-flops do not change state (no output).

t. Set the POWER switch to OFF. Disconnect the oscilloscope from the test set, and remove the flip-flop card from the F/F test jack.

25. Clock Pulse Generator Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for clock pulse generator testing:

a. Place clock pulse generator 532465 card into the CPG test jack on the front panel of the test set.

b. Set the POWER switch to ON.

c. Connect the trigger cable from the TRIGGER OUT jack on the test set to the trigger input jack on the oscilloscope. Set the TRIGGER switch to CLOCK PULSE, and synchronize the oscilloscope.

d. Insert the oscilloscope probe into test point CP and refer to E, figure 7, for the required waveform characteristics.

e. Set the POWER switch to OFF. Disconnect the oscilloscope from the test set, and remove clock pulse generator 532465 card from CPG test jack.

26. Core Register 9A Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for core register 9A testing:

a. Place core register 9A 531783 card into the C/RA test jack on the front panel of the test set.

b. Set the CORE REGISTER & CONDITION SELECTOR switch to 9 BIT–1.

c. Set the WORD SELECTOR switch to 1.

d. Set the POWER switch to ON. See that the OPERATE and ERROR lamps light.

e. Connect the trigger cable from the TRIGGER OUT jack on the test set to the trigger input jack on the oscilloscope. Set the TRIGGER switch to WORD, and synchronize the oscilloscope.

f. Press the RESET pushbutton. See that the ERROR lamp goes off.

g. Set the CORE REGISTER & CONDITION SELECTOR switch to 9 BIT–2. See that the ERROR lamp does not light.

h. Return the CORE REGISTER & CONDITION SELECTOR switch to 9 BIT–1. See that the ERROR lamp remains off.

i. If the ERROR lamp goes on, press the RESET pushbutton. See that the ERROR lamp goes off. If the ERROR lamp stays on, the core register is unsatisfactory.

j. Insert the oscilloscope probe into test point QA and refer to F, figure 7, for the required waveform characteristics.

k. Insert the oscilloscope probe into test point JA and refer to G, figure 7, for the required waveform characteristics.

l. Insert the oscilloscope probe into test point KA and refer to H, figure 7, for the required waveform characteristics.

m. Set the WORD SELECTOR switch to 2.

n. Insert the oscilloscope probe into test point QA and refer to I, figure 7, for the required waveform characteristics.

o. Insert the oscilloscope probe into test point JA and refer to J, figure 7, for the required waveform characteristics.

p. Insert the oscilloscope probe into test point KA and refer to K, figure 7, for the required waveform characteristics.

q. Set the WORD SELECTOR switch to 3.

r. Insert the oscilloscope probe into test point QA and refer to L, figure 7, for the required waveform characteristics.

s. Insert the oscilloscope probe into test point JA and refer to M, figure 7, for the required waveform characteristics.

t. Insert the oscilloscope probe into test point KA and refer to N, figure 7, for the required waveform characteristics.

u. Set the POWER switch to OFF. Disconnect the oscilloscope from the test set and remove core register 9A 531783 card from the C/RA test jack.

27. Core Register 10A Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for core register 10A testing:

a. Place core register 10A 531781 card into the C/RA test jack on the front panel of the test set.

b. Set the CORE REGISTER & CONDITION SELECTOR switch to 10 BIT–1.

c. Set the WORD SELECTOR switch to 1.

d. Set the POWER switch to ON. See that OPERATE and ERROR lamps light.

e. Connect the trigger cable from the TRIGGER OUT jack on the test set to the trigger input jack on the oscilloscope. Set the TRIGGER switch to WORD, and synchronize the oscilloscope.

f. Press the RESET pushbutton. See that the ERROR lamp goes off.

g. Set the CORE REGISTER & CONDITION SELECTOR switch to 10 BIT–2. See that the ERROR lamp does not light.

h. Return the CORE REGISTER & CONDITION SELECTOR switch to 10 BIT–1. See that the ERROR lamp remains off.

i. If the ERROR lamp goes on, press the RESET pushbutton. See that the ERROR lamp goes off. If the ERROR lamp stays on, the core register is unsatisfactory.

j. Insert the oscilloscope probe into the test point QA and refer to F, figure 7, for the required waveform characteristics.

k. Insert the oscilloscope probe into test point JA and refer to G, figure 7, for the required waveform characteristics.

l. Insert the oscilloscope probe into test point KA and refer to H, figure 7, for the required waveform characteristics.

m. Set the WORD SELECTOR switch to 2.

n. Insert the oscilloscope probe into test point QA and refer to I, figure 7, for the required waveform characteristics.

o. Insert the oscilloscope probe into test point JA and refer to J, figure 7, for the required waveform characteristics.

p. Insert the oscilloscope probe into test point KA and refer to K, figure 7, for the required waveform characteristics.

q. Set the WORD SELECTOR switch to 3.

r. Insert the oscilloscope probe into test point PA and refer to L, figure 7, for the required waveform characteristics.

s. Insert the oscilloscope probe into test point JA and refer to M, figure 7, for the required waveform characteristics.

t. Insert the oscilloscope probe into test point KA and refer to N, figure 7, for the required waveform characteristics.

u. Set the POWER switch to OFF. Disconnect the oscilloscope from the test set and remove core register 10A 531781 card from C/RA test jack.

28. Core Register 9B Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for core register 9B testing:

a. Place core register 9B 531784 card into the C/RB test jack on the front panel of the test set.

b. Set the CORE REGISTER & CONDITION SELECTOR switch to 9 BIT–1.

c. Set the WORD SELECTOR switch to 1.

d. Set the POWER switch to ON. See that the OPERATE and ERROR lamps light.

e. Connect the trigger cable from the TRIGGER OUT jack on the test set to the trigger input jack on the oscilloscope. Set the TRIGGER switch to WORD, and synchronize the oscilloscope.

f. Press the RESET pushbutton. See that the ERROR lamp goes off.

g. Set the CORE REGISTER & CONDITION SELECTOR switch to 9 BIT–2. See that the ERROR lamp does not light.

h. Return the CORE REGISTER & CONDITION SELECTOR switch to 9 BIT–1. See that the ERROR lamp remains off.

i. If the ERROR lamp goes on, press the RESET pushbutton. See that the ERROR lamp goes off. If the ERROR lamp stays on, the core register is unsatisfactory.

j. Insert the oscilloscope probe into test point QB and refer to F, figure 7, for the required waveform characteristics.

k. Insert the oscilloscope probe into test point JB and refer to G, figure 7, for the required waveform characteristics.

l. Insert the oscilloscope probe into test point KB and refer to H, figure 7, for the required waveform characteristics.

m. Set the WORD SELECTOR switch to 2.

n. Insert the oscilloscope probe into test point QB and refer to I, figure 7, for the required waveform characteristics.

o. Insert the oscilloscope probe into test point JB and refer to J, figure 7, for the required waveform characteristics.

p. Insert the oscilloscope probe into test point KB and refer to K, figure 7, for the required waveform characteristics.

q. Set the WORD SELECTOR switch to 3.

r. Insert the oscilloscope probe into test point QB and refer to L, figure 7, for the required waveform characteristics.

s. Insert the oscilloscope probe into test point JB and refer to M, figure 7, for the required waveform characteristics.

t. Insert the oscilloscope probe into test point KB and refer to N, figure 7, for the required waveform characteristics.

u. Set the POWER switch to OFF. Disconnect the oscilloscope from the test and remove core register 9B 531784 from C/RB test jack.

29. Core Register 10B Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for core register 10B testing:

a. Place core register 10B 531782 card into the C/RB test jack on the front panel of the test set.

b. Set the CORE REGISTER & CONDITION SELECTOR switch to 10 BIT–1.

c. Set the WORD SELECTOR switch to 1.

d. Set the POWER switch to ON. See that the OPERATE and ERROR lamps light.

e. Connect the trigger cable from the TRIGGER OUT jack on the test set to the trigger input jack on the oscilloscope. Set the TRIGGER switch to WORD, and synchronize the oscilloscope.

f. Press the RESET pushbutton. See that the ERROR lamp goes off.

g. Set the CORE REGISTER & CONDITION SELECTOR switch to 10 BIT–2. See that the ERROR lamp does not light.

h. Return the CORE REGISTER & CONDITION SELECTOR switch to 10 BIT–1. See that the ERROR lamp remains off.

i. If the ERROR lamp goes on, press the RESET pushbutton. See that the ERROR lamp goes off. If the ERROR lamp stays on, the core register is unsatisfactory.

j. Insert the oscilloscope probe into test point QB and refer to F, figure 7, for the required waveform characteristics.

k. Insert the oscilloscope probe into test point JB and refer to G, figure 7, for the required waveform characteristics.

l. Insert the oscilloscope probe into test point KB and refer to H, figure 7, for the required waveform characteristics.

m. Set the WORD SELECTOR switch to 2.

n. Insert the oscilloscope probe into test point QB and refer to I, figure 7, for the required waveform characteristics.

o. Insert the oscilloscope probe into test point JB and refer to J, figure 7, for the waveform characteristics.

p. Insert the oscilloscope probe into test point KB and refer to K, figure 7, for the required waveform characteristics.

q. Set the WORD SELECTOR switch to 3.

r. Insert the oscilloscope probe into test point QB and refer to L, figure 7, for the required waveform characteristics.

s. Insert the oscilloscope probe into test point JB and refer to M, figure 7, for the required waveform characteristics.

t. Insert the oscilloscope probe into test point KB and refer to N, figure 7, for the required waveform characteristics.

u. Set the POWER switch to OFF. Disconnect the oscilloscope from the test set and remove core register 10B 531782 from C/RB test jack.

30. Core Driver Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for core driver testing:

a. Place core driver 530842 card into CD test jack on the front panel of the test set. Allow 1 minute for warm up.

b. Set the CORE DRIVER switch to NORM.

c. Set the POWER switch to ON. See that the OPERATE and ERROR lamps light.

d. Connect the trigger cable from the TRIGGER OUT jack on the test set to the trigger input jack on the oscilloscope. Set the TRIGGER switch to CLOCK PULSE, and synchronize the oscilloscope.

e. Insert the oscilloscope probe into each of the test points CD1 and CD2 and refer to 0, figure 7, for proper waveform characteristics.

f. Set the CORE DRIVER switch to MARG.

g. Repeat step *e* above.

h. Set the POWER switch to OFF. Disconnect the oscilloscope from the test set and remove core driver 530842 card from CD test jack.

31. Emitter Follower Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for emitter follower testing:

a. Place emitter follower 531706 card into E/F test jack on the front panel of the test set.

b. Set the WORD SELECTOR switch to 1.

c. Set the POWER switch to ON. See that the OPERATE and ERROR lamps light.

d. Connect the trigger cable from the TRIGGER OUT jack on the test set to the trigger input jack on the oscilloscope. Set the TRIGGER switch to WORD, and synchronize the oscilloscope.

e. Set the EMIT. FOL.-NEGATOR switch to the positions listed, and insert the oscilloscope probe into the corresponding test points and refer to A, figure 7, for waveform characteristics as follows:

EMIT. FOL.-NEGATOR switch positions	OUTPUT test points (emitter follower circuit outputs)
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8

f. Set the POWER switch to OFF. Disconnect the oscilloscope from the test set and remove emitter follower 531706 card from E/F test jack.

32. Negator Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for negator testing:

a. Place negator 531137 card into the NEG test jack on the front panel of the test set.

b. Set the WORD SELECTOR switch to 1.

c. Set the POWER switch to ON. See that the OPERATE and ERROR lamps light.

d. Connect the trigger cable from the TRIGGER OUT jack on the test set to the trigger input jack on the oscilloscope. Set the TRIGGER switch to WORD, and synchronize the oscilloscope.

e. Set the EMIT. FOL.-NEGATOR switch to the positions listed, and insert the oscilloscope probe into the corresponding test points and refer to B, figure 7, for waveform characteristics as follows:

EMIT. FOL.-NEGATOR switch positions	Test points (negator circuit outputs)
1	1
2	2
3	3
4	4
5	5
6	6

f. Set the POWER switch to OFF. Disconnect the oscilloscope from the test set and remove negator 531137 card from the NEG test jack.

33. Diode Card Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for diode card testing:

a. Place diode 531723 card into the DIODE test jack on the front panel of the test set so that the diodes are on the left side of the card.

b. Set the TRANSISTOR-OFF-DIODE switch to DIODE.

c. Set the DIODE switch to FWD.

d. Set the TENS switch to 0.

e. Set the UNITS switch to 0.

f. Set the POWER switch to ON. See that the OPERATE and ERROR lamps light.

g. See that the panel meter reads 20 microamperes (full scale).

h. Set the UNITS switch to 1 and be sure the panel meter reads not more than 6.5 microamperes.

i. Repeat step *h* above for positions 2, 3, 4, 5, 6, 7, 8, and 9 of the UNITS switch.

j. Set the DIODE switch to REV. and place the UNITS switch in position 9. See that the panel meter reads not more than 2.5 microamperes.

k. Repeat step *j* above for positions 8, 7, 6, 5, 4, 3, 2, and 1 of the UNITS switch.

l. Set the UNITS switch to 0.

m. Set the TENS switch to 1. See that the panel meter reads not more than 2.5 microamperes.

n. Set the UNITS switch to positions 1, 2, 3, 4, 5, 6, 7, 8, and 9; see that the panel meter reads not more than 2.5 microamperes for each position.

o. Set the DIODE switch to FWD. and place the UNITS switch in position 9. See that the panel meter reads not more than 6.5 microamperes.

p. Repeat step *o* above for the 8, 7, 6, 5, 4, 3, 2, 1, and 0 positions of the UNITS switch.

q. Set the TENS switch to 2. See that the panel meter reads not more than 6.5 microamperes.

r. Set the UNITS switch to positions 1, 2, 3, 4, 5, 6, 7, 8, and 9; see that the panel meter reads not more than 6.5 microamperes for each position.

s. Set the DIODE switch to REV. and place the UNITS switch in position 9. See that the panel meter reads not more than 2.5 microamperes.

t. Repeat step *s* above for positions 8, 7, 6, 5, 4, 3, 2, 1, and 0 of the UNITS switch.

u. Set the TENS switch to 3 and place the UNITS switch at 0.

v. See that the panel meter reads not more than 2.5 microamperes for positions 0 and 1 of the UNITS switch.

w. Set the DIODE switch to FWD. and place in the UNITS switch in position 1.

x. See that the panel meter reads not more than 6.5 microamperes for positions 0 and 1 of the UNITS switch.

y. Set the POWER switch and TRANSISTOR-OFF-DIODE switch to OFF. Remove the diode card from the DIODE test jack on the test set.

34. Individual Diode Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for individual diode testing:

a. Place the diode to be tested in the DIODE EXTERNAL clips.

***Caution:* Be sure the diode is inserted in the DIODE EXTERNAL clips with the cathode of the diode in the left hand clip. See figure 10 for diode markings.**

b. Set the TENS switch to 3.

c. Set the UNITS switch to 4.

d. Set the DIODE switch to FWD.

e. Set the TRANSISTOR-OFF-DIODE switch to DIODE.

f. Set the POWER switch to ON. See that the OPERATE and ERROR lamps light.

g. Check the panel meter forward current reading listed in table II for the diode under test.

Note. All the diodes listed in table II have a tolerance of ±40 percent.

Table II. Individual Diode Test Current Readings

Diode type	Panel meter readings (microamperes)	
	Forward	Reverse
1N55B	7.0	6.0
1N67A	9.5	3.2
1N91	1.5	Full scale.
1N93	1.6	Full scale.
1N100	4.0	4.5
1N270	3.5	3.5
1N279	3.5	1.5
1N281	4.0	7.0
1N429	Full scale	Full scale.
1N466	6.8	Full scale.
1N468	6.5	Full scale.
1N470A	6.5	Full scale.
1N537	6.0	0
1N539	6.0	0
1N540	6.2	0
1N629	8.0	0
1N1313A	6.8	11.5
650C7	7.2	Full scale.
651C0	7.0	Full scale.
651C6	7.5	Full scale.
652C9	7.3	Full scale.
652CB	7.3	Full scale.
653C9	7.2	14.8
HD2038	9.5	2.2
HD2184	3.5	1.0
HD2270	5.5	1.9
HD2271	7.2	5.5
HD6002	7.2	0
HD6007	6.6	0
SV1015	6.5	7.0

Note. The panel meter readings given in table II are obtained at temperatures ranging from 20° C. (68° F.) to 30° C. (86° F.).

h. Set the DIODE switch to REV. and check the panel meter reverse current reading listed in table II for the diode under test.

i. Set the POWER switch to OFF. Remove the diode from the DIODE EXTERNAL clips on the test set.

35. Transistor Dynamic Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for transistor dynamic testing:

a. Insert a transistor (any one of which is given in the following chart) into the appropriate NPN or PNP socket of the transistor dynamic test card.

Transistor	Type
904A	NPN
953	NPN
2N327A	PNP
2N495	PNP
T643	PNP
2N43A	PNP
2N123	PNP
2N167	NPN
2N183	NPN
HA5003	NPN
GT–183	NPN

b. Select another transistor to meet the PNP or NPN requirements of the remaining transistor test socket on the transistor dynamic test card.

c. With both transistors installed in the transistor dynamic test card, place the card into the F/F test jack on the front panel of the test set.

d. Set the LOAD switch to JK (MED).

e. Proceed as directed in paragraph 24*a* and *d* through *s*. When the test is completed, perform the following steps:

f. Set the POWER switch to OFF. Disconnect the oscilloscope from the test set and remove the transistor dynamic test card from the F/F test jack. Remove the transistors installed in the PNP and NPN test sockets on the transistors dynamic test card.

36. Transistor Static Test

Prepare the test set as instructed in paragraph 23 and perform the following steps for transistor static testing:

a. Place a transistor (any one listed in table III) into the TRANSISTOR TEST socket on the front panel of the test set.

b. Set the TRANSISTOR-OFF-DIODE switch to TRANSISTOR.

Caution: **To avoid damage to the transistor under test, make certain that the TRANSISTOR switch is in one of the NPN positions when NPN type transistors are tested, or in one of the PNP positions when PNP type transistors are tested.**

c. Set the POWER switch to ON. See that the OPERATE and ERROR lamps light.

d. Check the transistor as specified in table III. Panel meter readings given have a tolerance of ±10 percent.

Table III. Transistor Static Test Requirements

Transistor	TRANSISTOR switch setting	Panel meter reading (microamperes)
2N43	PNP–IEO	8
	PNP–ICO	11
2N43A	PNP–IEO	2.2
	PNP–ICO	3.2
2N123	PNP–IEO	1.1
	PNP–ICO	1.0
2N167	NPN–IEO	1.0
	NPN–ICO	.3
2N183	NPN–IEO	2.0
	NPN–ICO	2.0
2N327A	PNP–IEO	0
	PNP–ICO	0
2N495	PNP–IEO	0
	PNP–ICO	0
904A	NPN–IEO	full scale
	NPN–ICO	0
953	NPN–IEO	full scale
	NPN–ICO	0
FT–183	NPN–IEO	2.5
	NPN–ICO	1.2
HA5003	NPN–IEO	5.0
	NPN–ICO	5.0

Note. The panel meter readings given in table III are obtained at temperatures ranging from 20° C. (68° F.) to 30° C. (86° F.).

e. Set the POWER switch and TRANSISTOR-OFF-DIODE switch to OFF. Remove the transistor from the TRANSISTOR TEST socket on the front panel of the test set.

37. Stowing Test Set After Use

After operation, put away the test set as follows:

a. Disconnect the power cable from power jack J3 and from the SYSTEMS TEST VOLTAGES jack on the maintenance bench.

b. Roll the power and trigger cables and place them in the rear compartment of the test set.

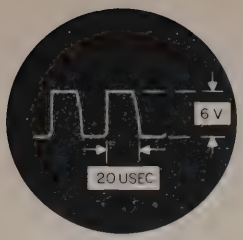
c. Shut the rear compartment door and fasten securely.

d. Replace the transistor dynamic test card in the clip fasteners on the inside of the cover.

e. Replace the cover on the test set and tighten all four thumbscrews.

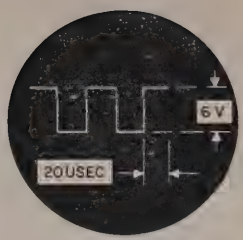
f. Replace the test set in the storage cabinets of the OC or CDG and secure in place with the web tiedown straps (fig. 3).

A TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 10 USEC
VOLTS/DIV 2



B TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 10 USEC
VOLTS/DIV 2

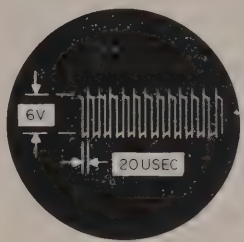
C TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 10 USEC
VOLTS/DIV 2



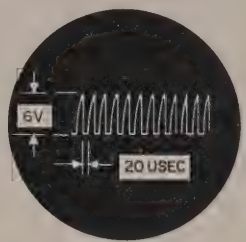
D TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 10 USEC
VOLTS/DIV 2

E TRIGGER SLOPE – INT
TRIGGER MODE DC
TIME/DIV 5 USEC
VOLTS/DIV 2

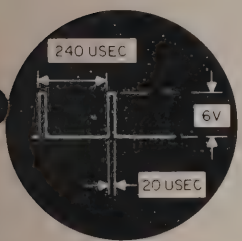
F TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 50 USEC
VOLTS/DIV 2



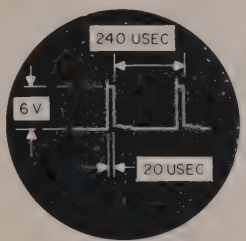
G TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 50 USEC
VOLTS/DIV 2



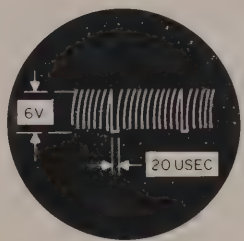
H TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 50 USEC
VOLTS/DIV 2



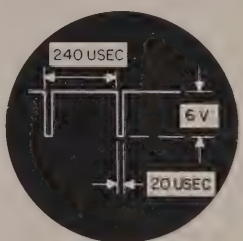
I TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 50 USEC
VOLTS/DIV 2



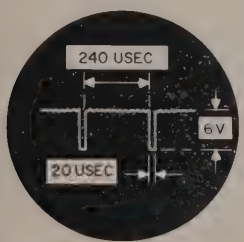
J TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 50 USEC
VOLTS/DIV 2



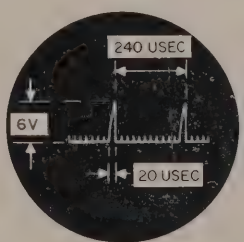
K TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 50 USEC
VOLTS/DIV 2



L TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 50 USEC
VOLTS/DIV 2



M TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 50 USEC
VOLTS/DIV 2



N TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV 50 USEC
VOLTS/DIV 2

O TRIGGER SLOPE + EXT
TRIGGER MODE DC
TIME/DIV .5 USEC
VOLTS/DIV 1

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Figure 7. Wave forms for plug-in circuit card tests.

CHAPTER 4

MAINTENANCE INSTRUCTIONS

38. Scope of First Echelon Maintenance

a. The maintenance duties normally performed by first echelon personnel for Test Set, Electronic Circuit Plug-In Unit TS–1209/MSQ do not require special tools or test equipment.

b. First echelon maintenance consists of the following:

(1) Preventive maintenance (par. 39).
(2) Visual inspection (par. 40).
(3) Operator's checklist (par. 41).

39. Preventive Maintenance

a. DA Form 11–266. DA Form 11–266 (figs. 8 and 9) is a preventive maintenance checklist to be used by the operator. Items not applicable to the test set are crossed out. References in the ITEM block contain additional information pertinent to the particular item. Instructions for use appear on the form.

b. Items. The information given below supplements DA Form 11–266. The item numbers correspond to the ITEM numbers on the form.

Item	Maintenance procedures
1	Use clean cloth to remove dust, dirt, moisture, and grease from cover, front panel, and exterior of case. If necessary, wet cloth with cleaning compound (Federal stock No. 7930–395–9542) and then wipe parts down with dry, clean cloth.
3	All control knobs should work smoothly, be tight on shafts, and should not bind. Tighten all loose knobs and make certain that knobs do not rub against front panel.
5	Repair any cuts in power cable insulation by covering them with rubber tape and then with friction tape.
7	All thumbscrews should work smoothly. Inspect threads and stops on thumbscrews for damage. Keep threads of thumbscrews clean and lightly lubricated with petroleum jelly. Inspect for missing hardware.

40. Visual Inspction

a. When the test set fails to perform properly, turn off the power and check all the items listed below. *Do not check any item with the power on.*

(1) Wrong settings of switches, controls, and adjustments.
(2) Power cable disconnected or poorly connected.
(3) Broken contacts of test jacks and sockets.

b. If the above checks do not locate the trouble, proceed to the operator's checklist.

41. Operator's Checklist

a. General. The operator's checklist will help the operator recognize a trouble quickly. If the normal indications are not observed, trouble-shooting at higher echelon is required. Note on the repair tag how the test set performed at the time of failure.

b. Procedure. Prepare the test set for operation as specified in paragraph 23. Perform the steps given in the operator's checklist in the order given.

c. Operator's Checklist.

Step	Action	Normal indication
1	Set POWER switch to ON___	OPERATE lamp lights. ERROR lamp lights.
2	Set TRANSISTOR-OFF-DIODE switch to TRANSISTOR. Set TRANSISTOR switch to CALIB.	Panel meter indicates 10 microamperes.
3	Set TRANSISTOR-OFF-DIODE to DIODE. Set TENS switch to 3 and UNITS switch to 2. Set DIODE switch to FWD.	Panel meter indicates 10 microamperes.
4	Set DIODE switch to REV. Set UNITS switch to 3.	Panel meter indicates 5 microamperes.

MAINTENANCE CHECK LIST FOR SIGNAL EQUIPMENT
TEST EQUIPMENT
(AR 750-625)

EQUIPMENT NOMENCLATURE

TEST SET, ELECTRONIC CIRCUIT PLUG-IN UNIT TS-1209/MSQ

EQUIPMENT SERIAL NUMBER 16

INSTRUCTIONS

This form may be used for a period of one month by using the correct dates and weeks of the month. It is to be used as a Preventive Maintenance check list for Signal equipment in actual use, or for a check on equipment prior to issue.

1. For detailed Preventive Maintenance instructions see:
   a. The Technical Manual *(in TM 11 series)* for the equipment. *(See DA Pamphlet Number 310-4)*
   b. The Supply Bulletin *(SB 11-100 series)* for the equipment. *(See DA Pamphlet Number 310-4)*
   c. The Department of the Army Lubrication Order. *(See DA Pamphlet Number 310-4)*

2. The following action will be taken by either the Communications Officer/ Chief for 1st echelon, or the Inspector for higher echelom
   a. Enter Equipment Nomenclature and Serial Number.
   b. Strike out items that do not apply to the equipment.

3. Operator/Inspector will enter in the columns entitled CONDITION, on the proper line, a notation regarding the condition, using symbols specified under LEGEND.

4. After operator completes each daily inspection he will initial over the appropriate dates under "Daily Condition for Month", then return form to his supervisor.

FOLD

TYPE OF INSPECTION

OPER-ATOR	2/3 ECH-ELON	DATE	SIGNATURE
✓		7 OCT. 59	Jack Jones

U. S. GOVERNMENT PRINTING OFFICE 1957 O—427138

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DA FORM 1 MAY 57 11-266

Figure 8. DA Form 11–266, pages 1 and 4.

LEGEND for marking conditions:
Satisfactory, ✓.
Adjustment, Repair or Replacement required, X.
Defect corrected, (X).

DAILY CONDITION FOR MONTH OF OCTOBER, 1959

NO.	DAILY ITEM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	2D 3D ECHELON
		17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
1.	CLEAN DIRT AND MOISTURE FROM EXPOSED SURFACES OF ~~HOUSINGS~~, CASES, CABINETS, CONTROL PANELS, INTERCONNECTING PLUGS, CABLES, ~~HEADSETS~~, METER WINDOWS, ETC. PAR. 39	✓	✓	✓	✓	✓	✓	✓											
2.	INSPECT FOR LOOSENESS OF EXTERIOR ITEMS SUCH AS SWITCHES, KNOBS, JACKS, CONNECTORS AND PILOT LIGHTS.	✓	✓	✓	Ø	✓	✓	✓										
3.	INSPECT CONTROLS FOR BINDING, SCRAPING. TAP CONTROLS LIGHTLY FOR CUT-OUT DUE TO LOOSE CONTACTS. PAR. 39	✓	✓	✓	✓	✓	✓	✓										
4.	DURING OPERATION BE ALERT FOR ANY UNUSUAL PERFORMANCE OR CONDITION.	✓	✓	✓	✓	✓	✓	✓										

WEEKLY	CONDITION EACH WEEK 1ST	2D	3D	4TH	5TH	2D 3D ECH
5. INSPECT CORDS, CABLES, WIRE ~~AND SHOCK MOUNTS~~ FOR BREAKS, CUTS, KINKS, DETERIORATION, STRAIN AND FRAYING. PAR. 39	✓					
6. ~~INSPECT CANVAS AND LEATHER ITEMS FOR FUNGUS, FRAYING, TEARS. BROKEN ZIPPERS AND SNAP FASTENERS.~~						
7. HAND CHECK FOR LOOSENESS OF EXTERIOR ITEMS SUCH AS HANDLES, LATCHES, HINGES. PAR. 39	✓					
8. ~~INSPECT FOR LUBRICATION IN ACCORDANCE WITH APPLICABLE DA LUBRICATION ORDER.~~						
9. ~~INSPECT DRY BATTERIES FOR DIRT, LOOSE TERMINALS AND LEAKAGE.~~						
10. INSPECT EXPOSED METAL SURFACES FOR RUST AND CORROSION.	✓					
11. INSPECT METERS FOR DAMAGED GLASS AND CASES.	✓					

ADDITIONAL ITEMS FOR 2D AND 3D ECHELON INSPECTIONS	CONDITION
12. ~~INSPECT SEATING OF READILY ACCESSIBLE ITEMS OF A PLUG-OUT NATURE; CRYSTALS, FUSES, CONNECTORS, PLUG-IN COILS, LAMPS, ETC. DO NOT REMOVE, ROCK OR TWIST TO INSPECT. USE ONLY A DIRECT PRESSURE TO INSURE THE ITEM IS FULLY SEATED.~~	
13. ~~INSPECT FOR CLEANLINESS AND TIGHTNESS OF SUCH ITEMS AS SHOCK MOUNTS, ANTENNA, ANTENNA MOUNTS AND WAVE GUIDES.~~	
14. ~~INSPECT RELAY AND CIRCUIT BREAKER ASSEMBLIES FOR DIRT, CORROSION, WORN OR BURNED CONTACTS.~~	

ADDITIONAL ITEMS FOR 2D AND 3D ECHELON INSPECTIONS	CONDITION
15. ~~INSPECT RESISTORS, BUSHINGS, INSULATORS FOR CRACKS, CHIPPING, BLISTERING, DISCOLORATION AND MOISTURE.~~	
16. ~~INSPECT JACKS AND CONNECTORS FOR SNUG FIT AND GOOD CONTACTS.~~	
17. ~~INSPECT VARIABLE CAPACITORS FOR DIRT AND MOISTURE.~~	
18. ~~INSPECT AIR FILTERS FOR CLEANLINESS.~~	
19. ~~INSPECT SCREWTYPE TERMINALS OF TRANSFORMERS, FIXED CAPACITORS, RESISTORS, CHOKES, POTENTIOMETERS AND RHEOSTATS FOR CORROSION, DIRT AND LOOSE CONTACTS.~~	
20. ~~CLEAN AND TIGHTEN SWITCHES, BLOWERS, RELAY CASES. CLEAN INTERIOR OF CHASSIS AND CABINETS.~~	
21. ~~INSPECT GENERATORS, MOTORS AND DYNAMOTORS FOR BRUSH WEAR, SPRING TENSION, ARCING AND COMMUTATOR WEAR.~~	
22. ~~INSPECT TERMINAL BLOCKS FOR LOOSE CONNECTIONS, CRACKS AND BREAKS.~~	
23. ~~INSPECT GASKETS AND BUSHINGS FOR WEAR AND DAMAGE.~~	
24. ~~INSPECT CATHODE RAY TUBES FOR BURNED SCREEN SPOTS.~~	
25. ~~BEFORE STORING OR SHIPPING REMOVE ALL BATTERIES.~~	

IF DEFICIENCIES NOTED ARE NOT CORRECTED DURING THE INSPECTION, INDICATE ACTION TAKEN FOR CORRECTION. *(Continue on page 4, if more space is needed)*

2 3

TM5895-244-10-9

Figure 9. DA Form 11-266, pages 2 and 3.

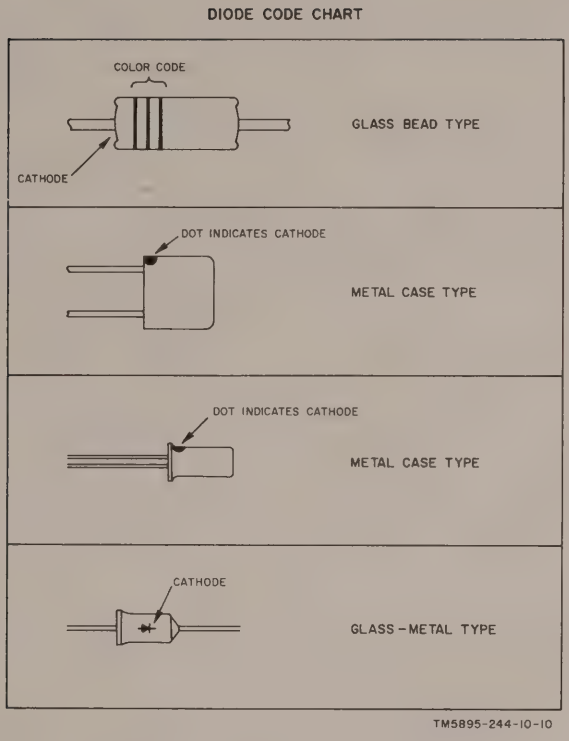

Figure 10. Crystal diode code chart.

CHAPTER 5

DEMOLITION TO PREVENT ENEMY USE

42. Authority for Demolition

The demolition procedures in paragraph 43 will be used to prevent the enemy from using or salvaging this equipment. Demolition of the test set will be accomplished only upon order of the commander.

43. Methods of Destruction

Any or all of the methods of destruction given below may be used. The time available will be the determining factor for the methods to be used in most instances when destruction of equipment is undertaken. The tactical situation also will determine in what manner the destruction order will be carried out.

a. Smash. Use sledges, axes, hammers, crowbars, and any other heavy tools available to smash the test set.

(1) Use the heaviest tools on hand to smash the front panel, test jacks and sockets, panel meter, and control knobs.

(2) If time permits, remove the five captive screws on the front panel and the seven captive screws on the rear panel and remove both panels. Use the heaviest tool on hand to smash the internal parts of the test set.

b. Cut. Use axes, handaxes, machetes, and similar tools to cut cabling, cording, and wiring. Use a heavy axe or machete to cut the power and trigger cables. Cut all cords, cables, and wiring in a number of places.

c. Burn. Burn the test set, using gasoline, oil, flame throwers, and similar tools. Burn the instruction literature first. Pour gasoline on cut cables and wiring and ignite.

***Warning:* Be extremely careful with explosives and incendiary devices. Use these items only when the need is urgent.**

d. Dispose. Bury or scatter destroyed parts or throw them into nearby waterways. This is particularly important if a number of parts have not been completely destroyed.

GLOSSARY

ac	alternating current
CD	core driver
CP	clock pulse
CPG	clock pulse generator
cps	cycles per second
CR	core register
C/RA	core register, A model
C/RB	core register, B model
dc	direct current
div	division
EF or EMIT. FOL.	emitter follower
EXT	external
F/F	flip-flop
FWD.	forward
INT	internal
kcs	kilocycles per second
NEG	negator
NORM.	normal
REV.	reverse
SENS.	sensitivity
STAB.	stability
time/div	time per division
usec or msec	microsecond
v	volt or volts
volt/div	volts per division

[AG 413.6 (20 Oct 59)]

By Order of *Wilber M. Brucker*, Secretary of the Army:

L. L. LEMNITZER,
General, United States Army,
Chief of Staff.

Official:

R. V. LEE,
Major General, United States Army,
The Adjutant General.

Distribution:

Active Army:

Def Atomic Spt Agcy (5)
USASA (2)
CNGB (1)
Tech Stf, DA (1) except
  CSigO (18)
Tech Stf Bd (1)
USA Arty Bd (1)
USA Armor Bd (1)
USA Inf Bd (1)
USA AD Bd (1)
USA Abn & Elct Bd (1)
USA Avn Bd (1)
USA ATB (1)
USCONARC (5)
US ARADCOM (2)
US ARADCOM Rgn (2)
OS Maj Comd (5)
OS Base Comd (5)
Log Comd (5)
MDW (1)
Armies (5) except
  First US Army (7)
Corps (2)
Div (2)
USATC (2)
Svc Colleges (5)
Br Svc Sch (5) except
  USASCS (25)
GENDEP (2) except
  Atlanta GENDEP (none)
Sig Sec, GENDEP (10)
Sig Dep (17)
Army Pictorial Cen (2)
Engr Maint Cen (1)
USA Ord Msl Comd (3)
USASSA (15)
USASSAMRO (1)
USA Sig Pub Agcy (8)
USA Sig Engr Agcy (1)
USA Comm Agcy (2)
USA Sig Eqp Spt Agcy (2)
USA Sig Msl Spt Agcy (13)
WRAMC (1)
AFIP (1)
AMS (1)
Ports of Emb (OS) (2)
Trans Terminal Comd (1)
Army Terminals (1)
OS Sup Agcy (1)
Yuma Test Sta (2)
USA Elct PG (1)
Sig Lab (5)
Sig Fld Maint Shops (3)
Mil Dist (1)
USA Corps (Res) (1)
Sector Comd, USA Corps (Res) (1)
JBUSMC (2)
Units org under fol TOE:
  11–7 (2)
  11–16 (2)
  11–57 (2)
  11–98 (2)
  11–117 (2)
  11–155 (2)
  11–500 (AA–AE) (2)
  11–557 (2)
  11–587 (2)
  11–592 (2)
  11–597 (2)

NG: State AG (3); units—same as Active Army except allowance is one copy to each unit.

USAR: None.

For explanation of abbreviations used, see AR 320–50.

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